

**REMARKS**

Reconsideration and allowance of this application are respectfully requested. New claim 9 has been added. Claims 6-8 have been canceled. Claims 1-5 and 9 are now pending in the application. The rejections are respectfully submitted to be obviated in view of the remarks presented herein.

**Rejection Under 35 U.S.C. § 103(a) - Khang et al in view of Sugio**

Claims 1-5 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Khang et al. (U.S. Patent Number 6,111,808; hereinafter “Khang”) in view of Sugio (U.S. Patent Number 5,602,796). The rejection is respectfully traversed.

Regarding claim 1, Applicants’ claimed invention relates to a semiconductor memory device comprising a plurality of subword drivers (SWDs) and a common inverter circuit. The plurality of subword driver circuits are commonly connected to a main word line and also connected to different subword selection lines. The common inverter circuit has an inverter input terminal and an inverter output terminal, the inverter input terminal being connected to the main word line and the inverter output terminal being connected to the plurality of driver input terminals. The subword driver circuits are each driven by a subword selection signal received through one of the subword selection lines.

Turning to the cited art, Khang describes a semiconductor memory device as shown in Figures 1 and 2a, including sub word line driver (SWD) sections (3) for driving memory cells in memory cell array sections (4), and row decoders (2) for generating a plurality of global word line bar (GWLb) signals and global word line (GWL) signals in the SWD sections (3) (column 1,

lines 22-27). The GWLb signals and the GWL signals are decoded by the most significant bit (MSB) address by row decoder (2) (column 1, lines 27-28).

Examiner maintains that the combination of Khang and Sugio teaches each feature of the claimed invention. However, Khang does not teach “a common inverter circuit having an inverter input terminal and an inverter output terminal, the inverter input terminal being connected to the main word line and the inverter output terminal being connected to the plurality of driver input terminals,” as Applicants claim. Khang’s row decoder (2) is not at all mentioned to include a common inverter circuit. Although it is shown in Figure 2a that row decoder (2) outputs a GWL signal and a GWLb signal, Khang does not disclose any relationship between GWL and GWLb. Examiner further contends that two transistors within the row detector (2) form a common inverter circuit, referring to the recitation in claim 4 of Khang. However, the two transistors disclosed by Khang is included in a data input/output controller (49) as shown in the separate circuit of Figure 4. Thus, Khang fails to teach a common inverter circuit and its specific connections to driver input terminals and a main word line, as recited in Applicants’ claim. Additionally, Khang fails to teach that the SWD sections (3) are commonly connected to the main word line. Furthermore, Examiner also readily admits in paragraph 6 of the Office Action that Khang discloses only a common subword selection signal (SWLE) connected to all the subword driver circuits instead of having each of the subword driver circuits driven by a subword selection signal received through one of the subword lines.

Sugio does not remedy the deficiencies of Khang. Sugio teaches a word line driver in a semiconductor memory device as shown in Figures 1 and 2. The word line driver (6) includes a

level shifter (40-1), and a plurality of groups of output units (50-1-1 through 50-1-m). The word line driver (6) serves as a circuit for selectively driving word lines  $WL_{1-1}$  through  $WL_{1-m}$  based on a group of decode signals A and word line activation signals  $PW_1$  through  $PW_m$  (column 2, lines 29-32).

However, there is also no teaching in Sugio of a common inverter circuit and its specific connections to driver input terminals and a main word line, as recited in Applicants' claim.

Additionally, although the group of decode signals A is input to the word line driver (6) as shown in Sugio's Figure 1, the input of A-1 to the level shifter (40-1) is not a main word line that is commonly connected to a plurality of subword driver circuits, as Applicants have claimed.

Each level shifter 40-1 receives its own separate input A-1 from the row address decoder (2). At least by virtue of the aforementioned differences, the invention defined by Applicants' claim 1 is patentable over Khang in view of Sugio. Applicants' claims 2-5 are dependent claims including all of the elements of independent claim 1, which, as established above, distinguishes over Khang in view of Sugio. Therefore, claims 2-5 are patentable over Khang in view of Sugio for at least the aforementioned reasons as well as for their additionally recited features.

Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

**Newly Added Claim**

Claim 9 is newly added by this Amendment and is believed to be in condition for allowance.

AMENDMENT UNDER 37 C.F.R. § 1.111  
U.S. Application No. 10/633,710  
Attorney Docket No. Q76859

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

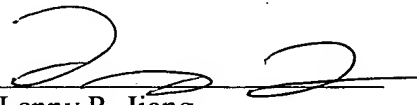
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**23373**

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Date: March 21, 2005

AMENDMENT UNDER 37 C.F.R. § 1.111  
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**AMENDMENTS TO THE DRAWINGS**

The attached sheet of drawings includes an amendment to FIG. 4 to replace the Japanese text with --quick change due to a small load--.

Attachment: Replacement Sheet (FIGS. 3 and 4)